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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:
Deshpande et al.

Serial No.: 10/709,048

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Group Art Unit: 2814

Examiner: Ingham, John C.

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Duane N. Moore

For: A MANUFACTURABLE METHOD AND STRUCTURE FOR DOUBLE SPACER
CMOS WITH OPTIMIZED NFET/PFET PERFORMANCE

RESPONSE UNDER 37 C.F.R. §1.111

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Commissioner for Patents
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Sir:

This is in response to the Office Action mailed October 24, 2006, setting a three-month
statutory period for response. Therefore, this response is timely filed.

10/709,048

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